

What is claimed is:

1. A method of manufacturing a semiconductor device,
comprising the steps of:

forming first and second active layers each formed of a
crystalline semiconductor film on an insulating surface of a
substrate;

making only said first active layer include an impurity
element that impart p-type conduction; and

subjecting said first and second active layers to a thermal
oxidization process in order that said impurity element is
incorporated into a thermal oxide film formed on a surface of
said first active layer;

wherein the element depthwise is said first active layer
active layer; and

wherein said distribution of concentration of said impurity
continuously reduced toward a main surface of in the vicinity of
the main surface of said first impurity element remaining in the
vicinity of the main surface of said first active layer is used
to control a threshold voltage.

2. A method of manufacturing a semiconductor device as

claimed in claim 1, wherein said first active layer constitutes a p-channel semiconductor device;

wherein said second active layer constitutes an n-channel semiconductor device; and

wherein said p-channel semiconductor device and said n-channel semiconductor device are complementarily combined with each other to form a CMOS structure.

3. A method of manufacturing a CMOS semiconductor device in which an n-channel semiconductor device and a p-channel semiconductor device are complementarily combined, said method comprising the steps of:

forming a first active layer comprising a crystalline semiconductor film including a p-type impurity and a second active layer on an insulating surface of a substrate, said second active layer not containing said -type impurity; and

subjecting said first and second active layers to thermal oxidization process to form a thermal oxide film thereon;

wherein said first active layer constitutes said p-channel semiconductor device, and said second semiconductor device constitutes said n-channel semiconductor device;

wherein said impurity element contained in said first active layer is incorporated into said thermal oxide film during said thermal oxidation process;

wherein the concentration of said impurity element in the main surface of said first active layer is reduced; and

wherein said impurity element remaining in the main surface of said active layer is used to control a threshold voltage.

4. A method of manufacturing a CMOS semiconductor device in which an n-channel semiconductor device and a p-channel semiconductor device are complementarily combined, said method comprising the steps of:

forming a first active layer and a second active layer each comprising a crystalline semiconductor film including a p-type impurity element on an insulating surface of a substrate;

subjecting said first and second active layers to a thermal oxidization process to form a thermal oxide film thereon;

wherein said first active layer constitutes said p-channel semiconductor device, and said second semiconductor device constitutes said n-channel semiconductor device;

wherein said impurity element contained in said first active layer are incorporated into said thermal oxide film through said thermal oxidation process;

wherein the concentration of said impurity element in the main surface of said first active layer is reduced; and

wherein said impurity element remaining in the main surface of said active layer is used to control a threshold value voltage.

5. A method of manufacturing a semiconductor device as claimed in claim 4, wherein said impurity element is added in a region including at least an edge portion in the active layer of said n-channel semiconductor device; and

wherein said impurity element is added in a region including no edge portion in at least a channel formation region in the active layer of said p-channel semiconductor device.

Sub B2 6. A method of manufacturing a semiconductor device as claimed in claim 1, wherein a thickness of said active layer is 100 to 1000 Å.

7. A method of manufacturing a semiconductor device as claimed in claim 2, wherein a thickness of said active layer is 100 to 1000 Å.

8. A method of manufacturing a semiconductor device as claimed in claim 3, wherein a thickness of said active layer is 100 to 1000 Å.

9. A method of manufacturing a semiconductor device as claimed in claim 4, wherein a thickness of said active layer is 100 to 1000 Å.

10. A method of manufacturing a semiconductor device as claimed in claim 5, wherein a thickness of said active layer is 100 to 1000 Å.

Sub B3
11. A method of manufacturing a semiconductor device comprising the steps of:

preparing a semiconductor island comprising crystalline silicon on an insulating surface;

introducing ions of an impurity comprising boron into said semiconductor island; and then

oxidizing a surface of said semiconductor island to form an oxide film so that a part of boron introduced into said semiconductor island is incorporated into said oxide film.

12. The method according to claim 1 wherein said semiconductor device is a liquid crystal display device.

13. The method according to claim 1 wherein said semiconductor device is an electroluminescent display device.

14. The method according to claim 1 wherein said semiconductor device is a video camera.

15. The method according to claim 1 wherein said semiconductor device is a personal computer.

16. The method according to claim 1 wherein said semiconductor is a projection system.

17. The method according to claim 3 wherein said semiconductor device is a liquid crystal display device.

18. The method according to claim 3 wherein said semiconductor device is an electroluminescent display device.

19. The method according to claim 3 wherein said semiconductor device is a video camera.

20. The method according to claim 3 wherein said semiconductor device is a personal computer.

21. The method according to claim 3 wherein said semiconductor device is a projection system.

22. The method according to claim 4 wherein said semiconductor device is a liquid crystal display device.

